Remarks

In the Office Action dated January 26, 2005, the Examiner rejected 23-26 under 35 U.S.C. § 103(a) as being unpatentable over *Snider* (U.S. Patent No. 5.991.893) in view of *Nikhil et al.* (U.S. Patent No. 5,499,349) and rejected claims 30-34 under 35 U.S.C. § 103(a) as being unpatenable over *Resman et al.* (U.S. Patent No. 5,535,364)[1] in view of *Nikhil et al.*

Based on the following remarks, Applicant respectfully traverses the rejection of claims 23-26 and 30-34 under 35 U.S.C. § 103(a).

I. The Information Disclosure Statements Filed January , 14, 2003, October 10, 2004, and January 28, 2005

Applicant has filed a number of Information Disclosure Statements (IDSs) since February 26, 2002. While the Examiner has provided copies of initialed PTO Form 1449s for most of the IDSs filed, Applicant has not received a copy of an initialed PTO Form 1449 for any of the IDSs filed January , 14, 2003, October 10, 2004, and January 28, 2005. Copies of the these IDSs and each corresponding stamped postcard showing receipt by the U.S. Patent and Trademark Office are attached. Applicant requests that the Examiner provide copies of initialed PTO Form 1449s and/or SB/08 associated with these IDSs indicating that the references listed therein have been considered by the Examiner.

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[1] The Examiner rejected claims 30-34 over "Resman et al. (USPN: 5,734,822)." That patent no., however, is issued to Houha et al. Applicant notes that Resman et al. corresponds to U.S. Patent No. 5,535,364, which was cited by the Examiner in the Form 892 accompanying the Office Action. As such, Applicant responds to the rejection of claims 30-34 under the assumption the Examiner intended to apply the '364 patent to Resman et al.

II. The Rejection of Claims 23-26

To establish a prima facie case of obviousness, three basic criteria must be met. First, the prior art reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. *See* M.P.E.P. § 2143.03. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. *See* M.P.E.P. § 2143. Third, a reasonable expectation of success must exist. *See* M.P.E.P. § 2143.02. Moreover, each of these requirements must "be found in the prior art, and not based on applicant's disclosure." M.P.E.P. § 2143.

In rejecting claim 23, the Examiner asserts the allocation table of the VRSM layer 101 disclosed by *Snider* corresponds to a memory designated for coordinating the assignment of the memory to one or more threads. (*See Office Action*, p. 3, lines 1-4.) Applicant disagrees. *Snider* describes a system where a number of distributed memories 106 make up a heap of memory from which a data structure 200 may be requested and used. (*See Snider*, col. 4, ll. 53-61 and col. 6, ll. 40-46.) The allocation tables taught by *Snider* are associated with the VRSM layer 101 that manages access to the data structure 200. Thus, the Examiner's assertion to that the allocation tables correspond to "an area of a memory," as recited in claim 23 is misguided. *Snider*'s allocation tables are not an area of a memory to which one or more threads require access. Instead, the tables are associated with VRSM layer 101. The memory heap is the shared memory used to generate the data structure 200 that is allocated for use by

the operating system, not memory areas reserved for VRSM operations. Accordingly, the Examiner's contention that "an area of *memory* designated for coordinating the assignment of *the memory* to one or more threads requiring access to *the memory*," as recited in claim 23, is disclosed by the allocation tables disclosed by *Snider* is not supported by the disclosure of that reference.

The Examiner also asserts that VRSM layer 101 includes usage information reflecting usage of "the memory." *Id.* at ll. 5-10. In particular, the Examiner asserts the memory size data associated with the data structure taken from the memory heap corresponds to usage information. Applicant disagrees. While *Snider* may supply information about a requested data structure (*See Snider*, col. 5, ll. 35-40.) none of this information reflects usage of "the memory," which, as explained above, the Examiner asserts is the allocation tables of the VRSM layer 101. Because the allocation tables are part of the VRSM layer 101, they cannot be not the same "memory" as the requested allocated data structure of the heap memory. Accordingly, the Examiner's contention that *Snider's* usage information corresponding to the requested data structure reflects usage of a "memory" that is designated for coordinating the assignment of "the memory," as recited in claim 23, is not supported by the reference.

The Examiner further asserts that *Snider* teaches "locking protocol or synchronizing protocol for serializing access to the memory by the one or more threads based on the usage information." (*See Office Action,* p. 3, ll.10-13.) Contrary to the Examiner's assertions, the processes taught by *Snider* that permit only one processor or thread to write to memory at one time, do not correspond to a protocol that serializes access to the memory based on the usage information. Accordingly, the Examiner's

contentions that *Snider* considers usage information when locking a memory for exclusive write purposes is unsupported by the reference.

Additionally, the Examiner admits that *Snider* fails to teach allowing a first thread to access a designated block of memory while another thread requests and secures access to another block. To address these deficiencies, the Examiner cites to *Nikhil et al.* In particular, the Examiner asserts that the pipelined operations disclosed by *Nikhil et al.* suggests to one skilled in the art to modify *Snider* as alleged in the Office Action. Applicant disagrees for the following reasons.

First, *Nikhil et al.* does not teach or even suggest the recitations that the Examiner admits are missing from *Snider. Nikhil et al.* merely discloses an instruction pipeline process where tokens are used as identifiers to facilitate an instruction fetch and execution stage of a pipeline. Nowhere does the reference discuss controlling or allocating memory or portions of a memory in the manner recited in claim 23. Instead, the token queue disclosed by *Nikhil et al.* stores instruction identifiers that are used as references that assist in maintaining consistent processing within an instruction pipeline 36.

Second, *prima facie* obviousness has not been established at least because there is no motivation to combine *Snider* and *Nikhil et al.* Determinations of obviousness must be supported by evidence in the record. *See In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001) (finding that the factual determinations central to the issue of patentability, including conclusions of obviousness by the Board, must be supported by "substantial evidence"). Further, the desire to combine references must be proved with "substantial evidence" that is a result of a "thorough and searching" factual inquiry.

In re Lee, 277 F.3d 1338, 1343-1344 (Fed. Cir. 2002) (quoting *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52).

In this case, the Office Action does not show that a skilled artisan considering *Snider* and *Nikhil et al.*, and not having the benefit of Applicant's disclosure, would have been motivated to combine or modify the references in a manner resulting in Applicant's claimed combination. In fact, the Examiner merely states a conclusion of the alleged combination without providing the requisite motivation to support the combination. The Examiner alleges that a skilled artisan would have modified *Snider* to "allow multiple operations be processed without having to wait for the completion of one operation in order to process the next, therefore enhancing system throughput.." (*See Office Action*, p. 4, ll. 16-19.) This conclusion is not properly supported and does not show that a skilled artisan would have combined the references as alleged. The mere fact that *Nikhil et al.* mentions a pipeline process does not show that a skilled artisan would have been motivated to modify *Snider* as alleged. Indeed, one of ordinary skill in the art would not have looked to an instruction level pipeline processing system, such as that taught by *Nikhil et al.*, for modifications to a distributed networked based system, such as that taught by *Snider*.

The M.P.E.P. makes clear that: "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination" M.P.E.P. § 2143.01 (citations omitted). The Examiner has not shown that the cited art "suggests the desirability" of the alleged combination. Indeed, there is no reason why a skilled artisan would look to modify *Snider*, which concerns shared memory allocation processes, with a instruction pipeline

system as disclosed by *Nikhil et al.* Therefore the conclusions in the Office Action were not reached based on facts gleaned from the cited references and that, instead, teachings of the present application were improperly used in hindsight to reconstruct the prior art. For at least these additional reasons, the Examiner has not established a *prima facie* case of obviousness with respect to claim 23, and thus, the rejection of that claim under 35 U.S.C. § 103(a) should be withdrawn.

Claims 24-26 depend from claim 23. As explained, the cited art does not support the rejection of claim 23. As such, the cited art does not support the rejection of claims 24-26 for at least the same reasons set forth in connection with the response to the rejection of claim 23. Further, the cited art does not teach or suggest the recitations of these claims as asserted by the Examiner. For example, the Examiner admits that the cited art does not teach the size of the designated memory being determined by a user. Nonetheless, the Examiner asserts such recitations are obvious without providing an evidence supporting the assertion. (*See Office Action,* p. 4, line 23- p. 5, l. 10.) As explained, conclusions of obviousness must be shown by substantial evidence. The Examiner has not pointed to any portion of the references that suggest the proposed combination. Instead, the Examiner presents an unsupported conclusion, such as alleging the proposed combination would allow the cited art to "serve [a] broader range of applications." These conclusions were not reached based on facts gleaned from the cited references. Accordingly, the Examiner has not established a *prima facie* case of obviousness with respect to claim 25, and thus, for this additional reason, the rejection of that claim under 35 U.S.C. § 103(a) should be withdrawn.

Further, the Examiner fails to address the recitations of claim 26. Nowhere does the Office Action address a designated block of memory being adjacent to a designated block of memory, as recited in claim 26. Indeed, the cited art fails to teach or suggest these recitations. For instance, *Snider* teach a distributed memory system that creates a shared memory heap from separate memories 106. The reference does not suggest that the requested data structure is adjacent to another memory area associated with another thread's access to the memory. Further, *Nikhil et al.* fails to address blocks of memories in an allocation system, much less adjacent blocks of memory. Accordingly, because the Examiner fails to address the recitations of claim 26, and the cited art fails to teach or suggest them, Applicant submits the rejection to claim 26 is improper and should be withdrawn.

III. The Rejection of Claims 30-34

The Examiner asserts *Resman et al.* teaches allocating to a first process, without accessing an operating system, a first block of memory that has a size designated by a user, as recited in claim 30. (*See Office Action,* p. 5, ll. 16-23.) In particular, the Examiner alleges that the allocation of a higher priority procedure (i.e., an application task) to a the AI/O RAM pool when the free RAM pool is full suggest the above recitations. *Id.* The Examiner further asserts that *Resman et al.* teaches allocating to a second process, without accessing an operating system, a second block of memory that has a size designated by a user. *Id.* at p.6, ll. 1-5.) Applicant disagrees with the Examiner's interpretation of *Resman et al.*

Resman et al. discloses a memory allocation system that allows applications to request and receive RAM space from a free RAM pool. If no space is available, an application is allowed access to a AI/O RAM pool. (*See Resman et al.*, col. 3, ll. 29-49.) I/O tasks are allocated space in an I/O fixed buffer pool. An I/O task may be allocated space in the AI/O RAM pool only when a certain amount of space is available in the free RAM pool. *Id.* at col. 3, ll. 50-62.

Contrary to the Examiner's assertions, *Resman et al.* does not teach or suggest allocating, without accessing an operating system, a first block of memory having a size designated by a user. The reference does not state that the size of any portion of the RAM pools are designated by a user. On the contrary, *Resman et al.* states that requests for RAM allocation are caused by an application running in CPU 14. (*See Resman et al.*, col. 3, ll. 29-30.) This software based allocation process does not provide for user input, much less input to designate a size of a block of memory to be allocated to a process. Further, the mere fact that *Resman et al.* allows an I/O task to access memory does (under certain conditions) does not bolster the Examiner's arguments. As explained, *Resman et al.* does not mention or disclose a user designated size of block of memory that is allocated without accessing an operating system to a first or second process.

The Examiner admits that *Resman et al.* does not teach allocating a second block of memory to the second process while the first process is accessing the first block of memory, as recited in claim 30. (*See Office Action*, p. 6, ll. 6-12.) To make up for these deficiencies, the Examiner again refers to the instruction pipeline system of *Nikhil et al.* Applicant disagrees with the Examiner's interpretation of the cited art.

As explained, *Nikhil et al.* merely discloses an instruction pipeline process where tokens are used as identifiers to facilitate an instruction fetch and execution stage of a pipeline. Nowhere does the reference discuss controlling or allocating memory or portions of a memory in the manner recited in claim 30. Instead, the token queue disclosed by *Nikhil et al.* stores instruction identifiers that are used as references that assist in maintaining consistent processing within an instruction pipeline 36. Accordingly, contrary to the Examiner's assertions, *Nikhil et al.* does not teach or suggest allocating a second block of memory to the second process while the first process is accessing the first block of memory, as recited in claim 30.

Additionally, the requisite motivation to combine *Resman et al.* and *Nikhil et al.* is lacking. As explained, determinations of obviousness must be supported by evidence in the record. The Examiner again does not show that a skilled artisan considering *Resman et al.* and *Nikhil et al.*, and not having the benefit of Applicant's disclosure, would have been motivated to combine or modify the references in a manner resulting in the recitations of claim 30. In fact, the Examiner presents the same reasons for combining *Nikhil et al.* with *Resman et al.* as those set forth in the rejection of claim 23 in view of *Snider* and *Nikhil et al.* (*See Office Action*, p. 4, ll. 8-21 and p 6, l. 13 to p. 7, l. 10.) The Examiner's conclusion is not properly supported and does not show that a skilled artisan would have combined the references as alleged. The mere fact that *Nikhil et al.* mentions a pipeline process does not show that a skilled artisan would have been motivated to modify *Resman et al.* as alleged. Indeed, one of ordinary skill in the art would not have looked to an instruction level pipeline processing system, such as

that taught by *Nikhil et al.,* for modifications to a memory allocation system within a printer processing system, such as that taught by *Resman et al.*

For at least these reasons, the Examiner has not established a *prima facie* case of obviousness with respect to claim 30, and thus, the rejection of that claim under 35 U.S.C. § 103(a) should be withdrawn and the claim allowed.

Claims 31-34 depend from claim 30. As explained, the cited art does not support the rejection of claim 30. As such, the cited art does not support the rejection of claims 31-34 for at least the same reasons set forth in connection with the response to the rejection of claim 30. Accordingly, Applicant requests that the rejection of these claims be withdrawn and the claims allowed.

IV. Conclusion

In view of the foregoing remarks, Applicant submits that this claimed invention, is neither anticipated nor rendered obvious in view of the cited art. Applicant therefore requests the Examiner's reconsideration and reexamination of the application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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